

Patent Application of James J. D'Amato, P.E. for "Bi-directionally Driven Forward Converter for Neutral Point Clamping in a Modified Sine Wave Inverter" continued

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CLAIMS

What is claimed is:

1. A method by which the output of a half bridge converter when used in producing a modified sine wave is clamped to a midpoint level between the voltages used within thereby providing an output waveform that remains consistent and independent of any given load.
2. A transformer with two primary windings magnetically coupled to one secondary winding wherein each said primary winding has current passing within it when its respective three terminal device closes the circuit.
3. The transformer of claim 2 wherein both of the said primary windings have an identical quantity of turns, are wound in an opposing manner to one another and the said secondary winding is wound with the same sense of only one said primary winding.
4. The transformer of claim 2 wherein each said primary winding is magnetically coupled to the common said secondary winding and for each positive voltage alternately induced across each said primary winding will produce a positive voltage across the common said secondary winding thereby declaring that the said transformer is operating in the forward converter mode.
5. The said secondary winding of claim 2 wherein its output is rectified, filtered, and connected to the source input of the said inverter thereby creating a non dissipative load with efficient utilization of transformed energy and simultaneously reflecting back to the said primary winding a low impedance for actively snubbing transients incurred by an output inductive load.

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6. Two independent directional diodes both connected to the load whereby only one said diode of the two at any instance of time permits current flow through its respective said primary winding of the said transformer mentioned in claim 2 and pending the polarity of the output waveform of the output said modified sine wave.
7. A high frequency snubber pulse generator that provides two outputs for their respective two inputs of which each output provides more than 50 pulses and less than 500 pulses coincidental with the dead time of the said modified sine wave output.
8. The high frequency snubber pulse generator of claim 7 wherein it contains a self oscillating circuit that outputs a succession of identical said pulses at a duty cycle no greater than fifty percent and for each said pulse provide transition times with very high slew rates in order to sustain the said pulse wave shape.
9. The high frequency snubber pulse generator of claim 7 wherein the supply voltage and return used for creating self oscillation be obtained from the input source voltage to the said inverter yet provide power and ground isolation when driving the said three terminal devices that support each said primary winding of the said transformer of claim 2.
10. The high frequency snubber pulse generator of claim 7 wherein it contains an output drive that can support the controlling terminal in the said three terminal device without distortion to the said output pulses and result with enough current flow through each said primary winding of the said transformer of claim 2 so as to allow the ramping current attain its final value.
11. The high frequency snubber pulse generator of claim 7 wherein the succession of identical said output pulses from either of the said two outputs is initiated and coincidental with the turning off of either of the two output power transistors used within the said half bridge converter.

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12. The high frequency snubber pulse generator of claim 7 wherein the output gating initiates the said output pulses from either of the said two outputs at a time no less than one half cycle of the output pulse frequency in order to accommodate turn off times of said either of the two output power transistors used within the said half bridge converter.
13. The high frequency snubber pulse generator of claim 7 wherein the said output gating initiates the sequence of the said output pulses in the low state with minimal delay when driving any said three terminal device.